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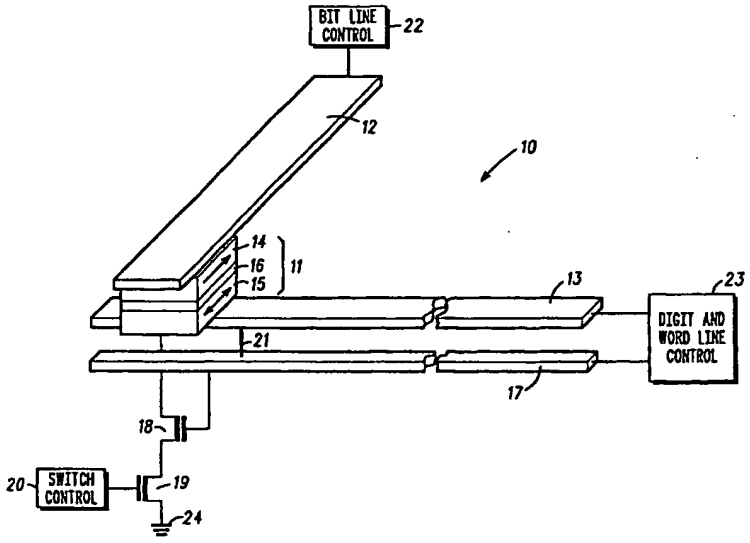

(57) Abstract

A high speed and high density magnetoresistive random access memory (MRAM) device (30) is provided. The MRAM device employs a poly-silicon word line (39a) that saves wiring space. Further, the word line is connected to a digit line (38a) by a connecting line (44a) which reduces an electrical resistance between transistors (43a and 40a). Arrangement of the connecting line reduces a transmission time from a digit current control (33a) to transistor (43a) and greatly improves a memory cycle time.

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MRAM WITH SHARED WORD AND DIGIT LINES

Field of the Invention

The present invention relates to a magnetoresistive random access memory having shared word and digit lines, and more particularly, to a magnetoresistive random access memory having a connecting line between word and digit lines.

Background of the Invention

A magnetoresistive random access memory (MRAM), which is one of non-volatile memory devices, includes a plurality of magnetic memory cells. It is known that the magnetoresistive effect appears in multi-layer films that are alternately stacked by magnetic layers and non-magnetic layers. Magnetic resistance over a magnetic memory cell indicates minimum and maximum values when magnetic vectors in magnetic layers point in same and opposite directions, respectively. The same and opposite directions of magnetic vectors in two magnetic layers are called "Parallel" and "Antiparallel" states, respectively. When magnetic material is employed for a memory device, parallel and antiparallel directions, for example, are logically defined as "0" and "1" states, respectively.

The MRAM device normally arranges magnetic memory cells on intersections of word and sense lines, which are placed in rows and columns. The MRAM circuit, for instance, is described in U.S. patent application No. 09/055,731 entitled "MAGNETORESISTIVE RANDOM ACCESS MEMORY DEVICE AND OPERATING METHOD THEREOF," filed April 1, 1998 assigned to the same assignee.

Activation of word and sense lines enables the MRAM device to access the memory cell. The sense line is

device to access the memory cell. The sense line is directly coupled to the memory cells and a sense current flows in the magnetic layers so that a sense current is affected by magnetic vectors in the magnetic layers and the sense current value in the memory cell or the voltage drop across the memory cell is alternated according to the direction of magnetic vectors. Sensing the changes in the sense current value or the voltage drop allows one to detect states stored in the memory cells. On the other hand, a writing process is carried out by applying a sufficient magnetic field to switch magnetic vectors in the magnetic layers. In order to meet the magnetic requirements, a torque or digit line is placed in parallel with the word line to provide a digit current. The digit, word, and sense currents all create a total magnetic field and apply it to the memory cell, which stores states in the memory cell in accordance with directions of the total magnetic field.

In order to ensure a sufficient current, digit, word, and sense lines typically employ metal material, which causes a memory cell size to increase for accommodation of all three metal spacing and pitches. Accordingly, a word line is replaced with poly-silicon material to alleviate a space limitation. Replacement to poly-silicon allows an MRAM device to highly integrate memory cells. A poly-silicon line, however, has an increased resistance that causes a transmission delay of a signal on the word line and requires much access time. Therefore, the more memory cells that are integrated, the more access time is needed.

Accordingly, it is a purpose of the present invention to provide an improved MRAM device that has a high-speed operation.

It is another purpose of the present invention to provide an improved MRAM device that has a high density memory cell arrangement.

It is still another purpose of the present invention to provide an improved MRAM device that attains reduction in memory cell size.

Summary of the Invention

These needs and others are substantially met through provision of a magnetoresistive random access memory (MRAM) device that includes connecting lines coupling between a digit line and a word line. The MRAM device has a plurality of memory cells arrayed in rows and columns. Each memory cell is placed on an intersection of a sense or bit line and a digit line. A word line, which is formed of poly-silicon material, is arranged in parallel with the digit line. The word line connects a plurality of memory cells arranged in a row that form a memory bank. Connecting lines are connected between the digit line and the word line at every N memory cells in the memory bank. The number N is a positive integer. The connecting lines reduce the access time to the memory cell because shared word and digit lines decrease the resistance. Accordingly, connecting lines formed between the word line and the digit line reduce a memory cell size, and highly improve the access time to memory cells.

Brief Description of the Drawings

FIG. 1 shows a simplified and schematic circuit diagram for describing a basic concept according to the present invention;

FIG. 2 shows an MRAM device circuit employing the present invention; and

FIG. 3 shows another embodiment for a memory bank circuit in an MRAM device.

Detailed Description of the Preferred Embodiments

FIG. 1 shows a simplified and schematic circuit diagram 10 that has a magnetic tunneling junction (MTJ) memory cell 11 placed on an intersection of a bit line 12 and a digit line 13. Memory cell 11 has three layers that include magnetic layers 14 and 15 separated by a non-magnetic and insulated layer 16. Insulated layer 16 is very thin and has typically a thickness of 10Å to 30Å that forms a tunneling junction between magnetic layers 14 and 15. Magnetic layer 14 is electrically connected to bit line 12 for providing a sense current to memory cell 11. As shown in FIG. 1, for example, memory cell 11 has magnetically pinned and free layers 14 and 15, respectively. Magnetic layer 15 stores information as directions of magnetization vectors therein. A word line 17 is placed in parallel with digit line 13 and is connected to a gate electrode of a memory cell transistor 18. Transistor 18 is connected to layer 15 and a ground switch transistor 19 that is controlled by ground switch control 20. A connecting line 21, which is formed of a metal such as Al, Cu, or TiW, electrically connects digit line 13 to word line 17. Bit line 12 is connected to a bit line control 22, while digit and word lines 13 and 14 are connected to digit and word line control 23. Bit line control 22 and digit and word line control 23 control current flow in bit line 12, digit line 13, and word line 17 on read and write modes. It is understood that the magnetic memory cell can be any combination of magnetic layers sandwiched of an insulator (MTJ) or magnetic layers sandwiched of a conductive layer.

In order to read information stored in memory cell 11, digit and word line control 22 sends a word signal on both word line 17 and digit line 13 that permits transistor 18 to turn on. At the same time, ground switch control 20 turns transistor 19 on. Then, bit line control 22 provides a sense current on bit line 12, which

flows through memory cell 11, transistors 18 and 19 to a ground or common line 24. The sense current generates a voltage drop across memory cell 11, which varies according to information in cell 11, that is "Parallel" and "Antiparallel" states. A comparator circuit (not shown) measures the voltage drop and determines states stored in memory cell 11.

Bit line 12 and digit line 13 are both formed by a metal such as aluminum or copper, whereas word line 17 is made of poly-silicon that has higher resistivity than metals. If only word line 17 carries the word signal to transistor 18, the signal transmission is delayed to transistor 18 due to the resistance of word line 17. This means the access time to memory cells greatly increases. In the present invention, connecting line 21 connects digit line 13 to word line 17 so that the resistance between control 23 and transistor 18 is reduced because digit line 13 is made of a metal. Accordingly, the word signal reaches transistor 18 without delay caused by poly-silicon in word line 17.

In a write mode, a bit current and a digit current are provided on bit line 12 and digit line 13, respectively. These currents generate magnetic fields that produce a combined magnetic field. The combined magnetic field has a sufficient magnetic strength to switch magnetic vectors in magnetic layer 15. The writing process carries out the following steps. First of all, ground switch control 20 turns off transistor 19 to avoid current flow from bit line 12 through memory cell 11 and transistors 18 and 19 to common line 24. Next, bit line control 22 provides a bit current on bit line 12 and digit and word line control 23 gives a digit current on digit line 13. Bit and digit lines 12 and 13 designate memory cell 11, to which the combined magnetic field is applied to store or switch states in magnetic layer 15.

Referring to FIG. 2, an MRAM device 30 is illustrated, which arranges a plurality of MTJ memory cells in rows and columns. Device 30 is roughly divided into a memory array 31 and a peripheral circuit portion including a bit line control 32, digit current controls 33a and 33b, a digit selector 34, and a switch control 35. Memory array 31 has a plurality of memory cells 36a and 36b (Not numbering all the cells and other elements in FIG. 2.) that are located on intersections of bit lines 37a and 37b and digit lines 38a and 38b. Bit line control 32 extends bit lines 37a on memory array 31 and 37b that are coupled to memory cells 36a and 36b. Digit lines 38a and 38b are coupled to transistors 40a-40d, one of which is selected by digit line selector 34 to supply a digit current. Transistors 40a and 40b further are coupled to transistors 41a and 41b, which determine directions of the digit current along with transistors 42a and 42b under the control of digit current controls 33a and 33b. Word lines 39a and 39b are placed in parallel with digit lines 38a and 38b, and coupled to gate electrodes of transistors 43a and 43b. Connecting lines 44a and 44b electrically connect between digit line 38a and word line 39a, and between digit line 38b and word line 39b. In memory array 31 in FIG. 2, connecting lines 44a and 44b are placed at every two memory cells in rows. Transistors 45a and 45b, which are controlled by switch control 35, connect transistors 43a and 43b to a ground or common line 46.

A reading operation for device 30 basically executes the same steps as the operation of the schematic circuit diagram 10 illustrated in FIG. 1. The following steps describe a reading operation to memory cell 36a, for example, where transistors 43a and 45a and connecting line 44a correspond to transistors 18 and 19 and connecting line 21 in circuit diagram 10 in FIG. 1, respectively.

First of all, digit line selector 34 provides a signal on a line 46 to turn on transistor 40a, by which digit line 38a is activated. Next, to turn on transistor 43a, digit current control 33a turns transistor 41a on and transistor 41b off. As a result, a digital high voltage on a power line 47 is applied through transistor 41a, transistor 40a, digit line 38a and connecting line 44a to the gate electrode of transistor 43a. Finally, switch control 35 sends a turn-on signal to transistor 45a, which allows a sense current to travel from bit line control 32 through bit line 37a, memory cell 36a transistor 43a, and transistor 45a to common line 46. The sense current generates a voltage drop across memory cell 36a, which is evaluated by a comparator circuit (not shown) to determine states stored in memory cell 36a.

As mentioned earlier, a combined magnetic field determines directions of magnetic vectors in the memory cell and stores states therein. In device 30, current flow directions in a digit line establish states in the memory cell. For example, it is assumed that digit currents on line 38a flowing to the right and left directions indicated by arrows 49 and 50 store a logic "0" and a logic "1" in the memory cell, respectively.

For writing a logic "0" in memory cell 36a, digit line selector 34 turns on transistor 40a to activate digit line 38a. Switch control 35 turns off transistor 45a to keep a current from flowing in memory cell 36a before bit line control 32 provides a bit current on bit line 37a. Then, current control 33a switches transistor 41a to turn off and transistor 41b to turn on, while current control 33b turns transistor 42a on and transistor 42b off. Consequently, the digit current indicated by arrow 49 flows from a power line 51 through transistor 42a, digit line 38a, transistor 40a, and transistor 41b to common line 46. A magnetic field generated by the digit current on digit line 38a is

combined with a magnetic field generated by the bit current on bit line 37a to produce a combined magnetic field that determines the direction in magnetic vectors in memory cell 36 and stores the logic "0."

Alternatively, in order to store a logic "1," a digit current represented by arrow 50 is provided in digit line 38a. First, digit line selector 34 selects digit line 38a by turning on transistor 40a, while transistor 45a is shut off. Digit current control 33a allows transistors 41a and 41b to turn on and off, respectively. At the same time, transistors 42a and 42b are turned off and on by current control 33b, respectively. As a result, a digit current route, which is from power line 47 through transistor 41a, transistor 40a, digit line 38a, and transistor 42a to common line 46, is formed. Bit line control 32 provides a bit current on bit line 37a, which forms a combined magnetic field along with a magnetic field generated by the digit current.

In FIG. 2, memory cell 36a is connected to transistor 43a in series, which forms a memory element. Each digit line, to a row direction, has a plurality of memory elements, which is called a memory bank. That is, memory array 31 includes a plurality of memory banks, each memory bank is activated by digit line selector 34. Memory banks shown in FIG. 2 have connecting lines 44a and 44b that are formed at every two memory elements in memory banks.

Referring to FIG. 3, another circuit configuration is illustrated for a memory array 60. A memory bank 61, for example, has a plurality of memory elements in parallel, and each memory element has a memory cell and a transistor connected in series. These memory cells position on intersections of a plurality of bit lines 62 and a digit line 63. A word line 64 is placed in parallel with digit line 63. Memory bank 61 basically is

the same as the circuit in FIG. 2 except for the connecting lines. In memory bank 61, connecting lines 65-67 are arranged at every 16 memory elements for connecting digit line 63 to word line 64. Generally speaking, connecting lines are placed between the digit line and the word line at every N memory elements, where the N is a positive integer number and is determined according to electrical resistivity of a word line.

Thus, a word line employs poly-silicon that allows an MRAM device to save space for wiring and to increase memory density. Furthermore, since connecting lines electrically connect a digit line to a word line at every N memory element, the resistance of the word line is substantially decreased along with a digit line, a memory access time is greatly improved and a total cycle for reading is highly reduced.

What is claimed is:

1. A magnetic random access memory unit comprising:

a memory element including:

a magnetic memory cell having first and second magnetic layers separated by a non-magnetic layer; and

a memory cell switch being connected in series to the magnetic memory cell for activating the magnetic memory cell;

a bit line being placed on the first magnetic layer and electrically coupled to the first magnetic layer;

a digit line being placed adjacent the memory cell, electrically isolated from the memory cell, and perpendicularly placed to the bit lines;

a word line being placed in parallel to the digit line and coupled to the memory cell switch for controlling the memory cell switch; and

a connecting line for electrically connecting the digit line to the word line.

2. The magnetic random access memory unit as claimed in claim 1 wherein the memory cell switch is a transistor having first, second and gate electrodes, the first electrode being coupled to the second magnetic layer, the second electrode being coupled to the ground switch, and the gate electrode being coupled to the word line.

3. The magnetic random access memory unit as claimed in claim 1 wherein, on a write mode, a bit current and a digit current are provided on the bit line and the digit line, respectively, so that the bit current and the digit current generate magnetic fields, respectively, a combined magnetic field of which determines directions of magnetic vectors in the magnetic memory cell.

4. The magnetic random access memory unit as claimed in claim 1 wherein the first magnetic layer is magnetically free and the second magnetic layer is magnetically pinned so that information is stored in the first layer as directions of magnetization vectors.

5. The magnetic random access memory unit as claimed in claim 1 wherein the magnetic memory cell has a tunneling junction between the first and second magnetic layers.

6. A magnetic random access memory bank comprising:

a plurality of memory elements, each memory element including:

a magnetic memory cell having first and second magnetic layers separated by a non-magnetic layer; and

a memory cell switch being connected in series to the magnetic memory cell for activating the magnetic memory cell;

a plurality of bit lines, each bit line being placed on the first magnetic layer and electrically coupled to the first magnetic layer;

a digit line being placed adjacent the memory cell, electrically isolated from the memory cell and perpendicularly placed to the bit lines;

a word line being placed in parallel to the digit line and coupled to memory cell switches for controlling the memory cell switches; and

a plurality of connecting lines for electrically connecting the digit line to the word line at every N memory elements, wherein the N is a predetermined positive integer number.

7. The magnetic random access memory bank as claimed in claim 6 further including a ground switch for coupling magnetic memory cells to a common line, wherein the ground switch is turned on for providing a sense current to one of the magnetic memory cells on a read mode.

8. The magnetic random access memory unit as claimed in claim 6 wherein, on a write mode, a bit current and a digit current are provided on one of the bit lines and the digit line, respectively, so that the bit current and the digit current generate magnetic fields, respectively, a combined magnetic field of which determines directions of magnetic vectors in the magnetic memory cell.

9. A magnetic random access memory device comprising:

a memory array including a plurality of memory elements arranged in rows and columns, each memory element having:

a magnetic memory cell including first and second magnetic layers separated by a non-magnetic layer; and

a memory cell switch being connected in series to the magnetic memory cell for activating the magnetic memory cell;

a plurality of bit lines, each bit line being placed on first magnetic layers of magnetic memory cells arranged in a column line and electrically coupled to the first magnetic layers;

a plurality of sets of digit and word lines, each set of digit and word lines having:

a digit line being placed adjacent memory cells arranged in a row line, electrically isolated from the memory cells, and perpendicularly placed to the plurality of bit lines; and

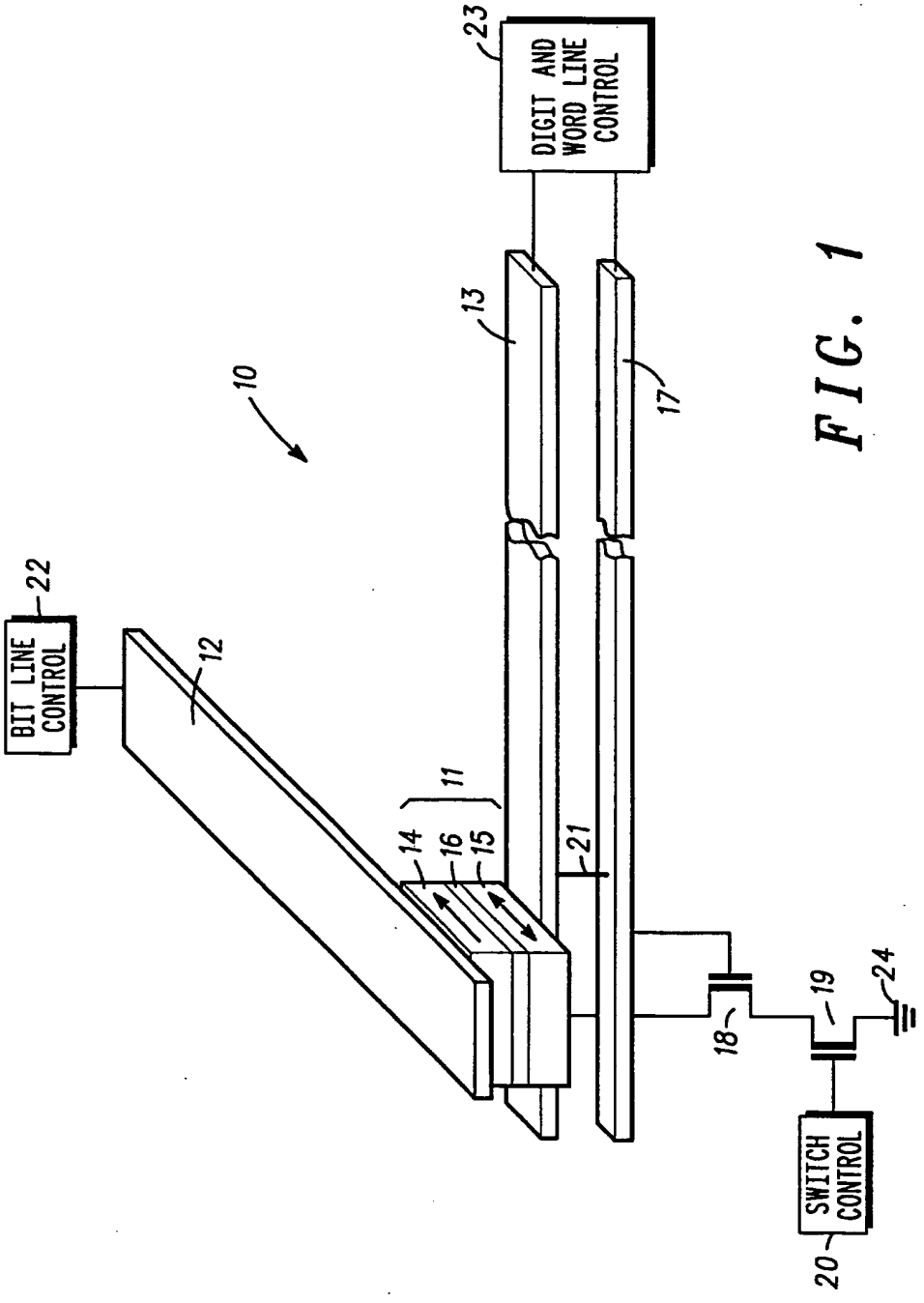
a word line being placed in parallel with the digit line and coupled to memory cell switches arranged in the row line for controlling the memory cell switches;

a plurality of sets of connecting lines, each set of connecting lines for electrically connecting between the digit line and the word line at every N memory elements in the row line, wherein the N is a predetermined positive integer number;

a bit line controller, coupled to the plurality of bit lines, for selecting one of the plurality of bit lines; and

a digit line controller, coupled to the plurality of digit lines, for selecting one of the plurality of digit lines.

10. The magnetic random access memory device as claimed in claim 9 wherein the bit line controller provides a bit current on one of the bit lines and the digit line controller provides a digit current on one of the digit lines, so that the bit current and the digit current generate magnetic fields, respectively, a combined magnetic field of which determines directions of magnetic vectors in the magnetic memory cell.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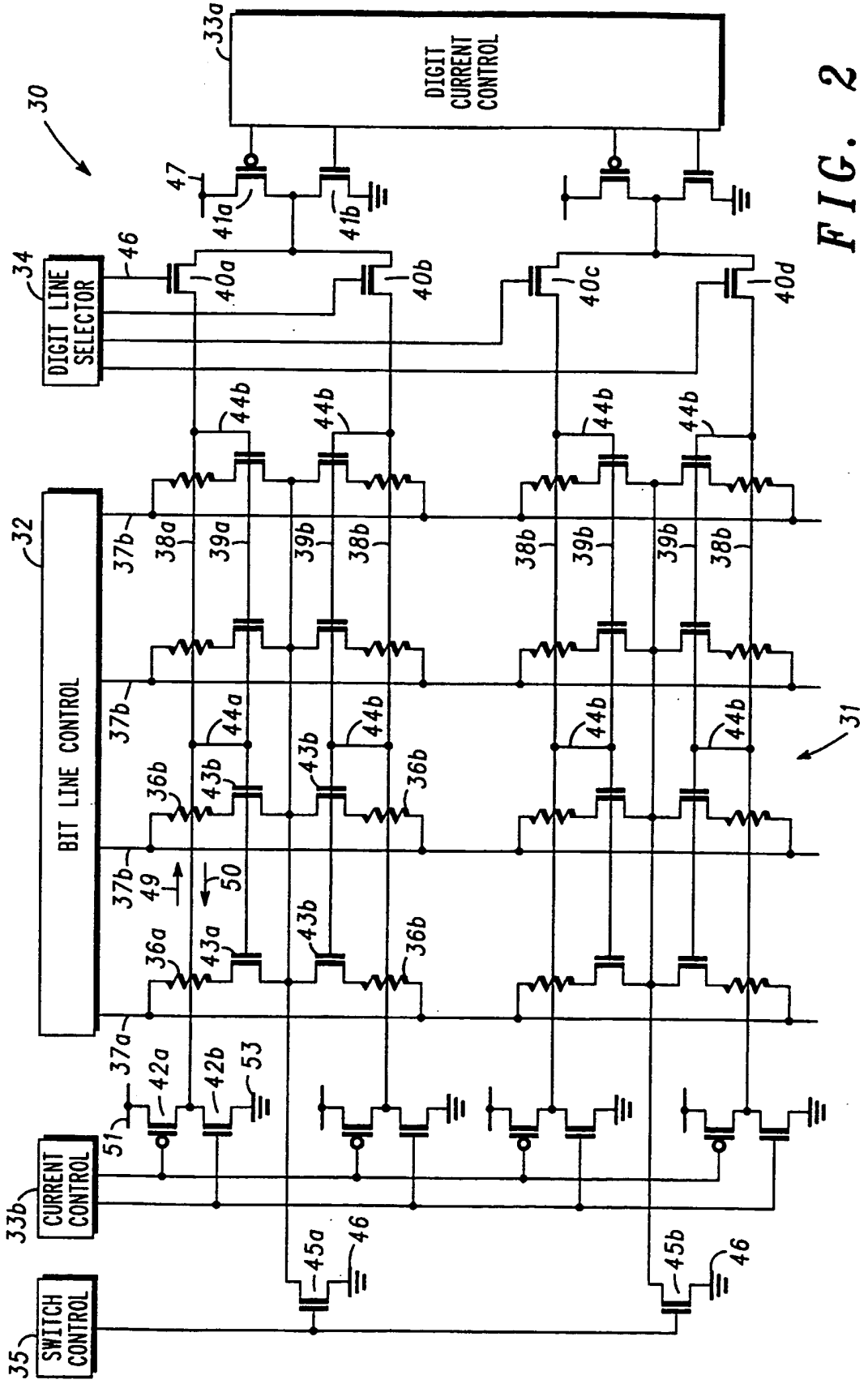
DIGIT AND WORD LINE CONTROL
13
17
10
22
BIT LINE CONTROL
12
11
14
16
15
21
18
19
24
SWITCH CONTROL
20

FIG. 1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33a
DIGIT CURRENT CONTROL
47
41a
41b
34
DIGIT LINE SELECTOR
46
40a
40b
40c
40d
44b
32
BIT LINE CONTROL
37b
38a
39a
39b
38b
44a
43b
36b
31
49
50
36a
43a
37a
42a
42b
53
51
33b
CURRENT CONTROL
45a
45b
35
SWITCH CONTROL

FIG. 2

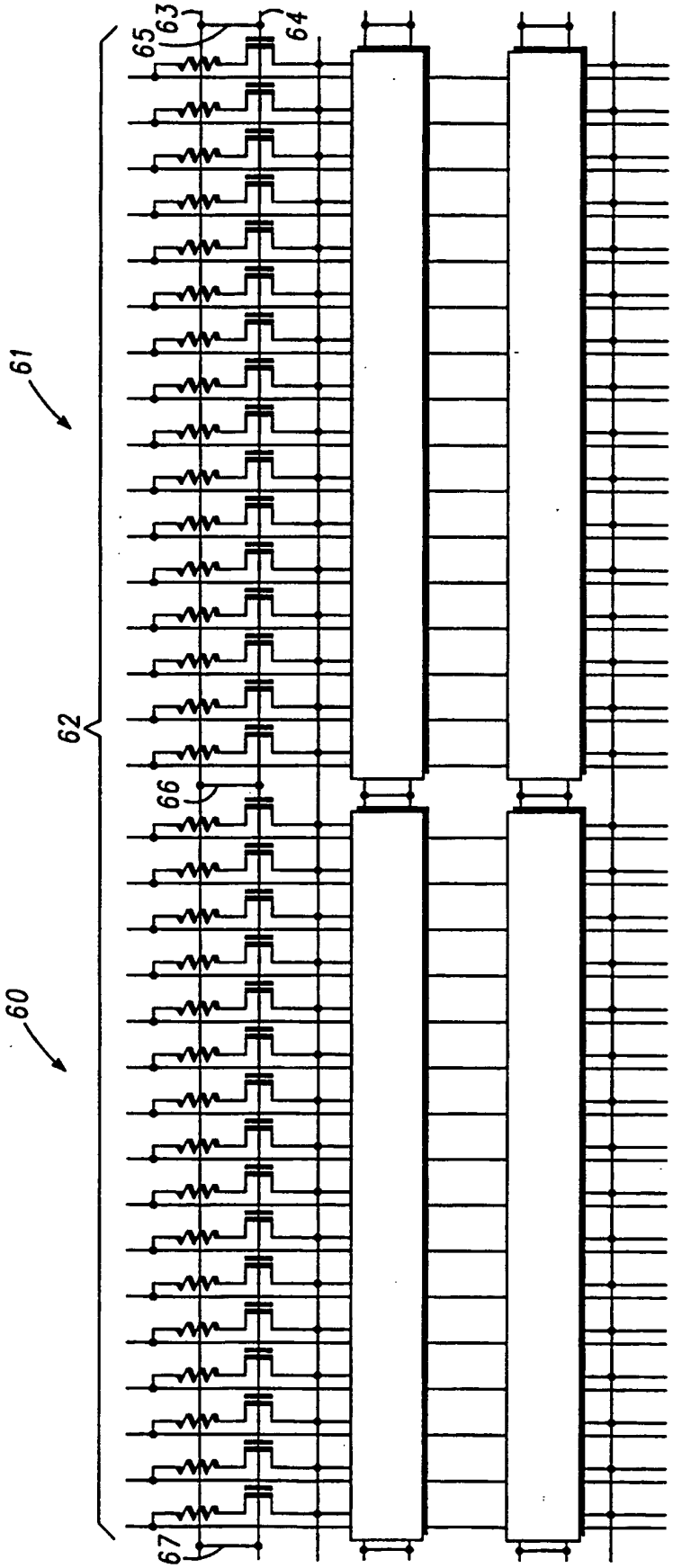

FIG. 3

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 99/16197

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G11C11/15 G11C11/16

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 541 868 A (PRINZ GARY A) 30 July 1996 (1996-07-30) column 5, line 3 -column 5, line 46 column 6, line 56 -column 6, line 67	1
A	US 5 173 873 A (WU JIIN-CHUAN ET AL) 22 December 1992 (1992-12-22) column 5, line 23 -column 6, line 27; figures 4,5	1
A	US 5 468 985 A (HARIMA TAKAYUKI) 21 November 1995 (1995-11-21) figure 1	1

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☒ Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
11 November 1999	17/11/1999

Name and mailing address of the ISA	Authorized officer
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 99/16197

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5541868 A	30-07-1996	NONE	
US 5173873 A	22-12-1992	NONE	
US 5468985 A	21-11-1995	JP 6318645 A	15-11-1994

a read access circuit (40) coupled to said memory cell (36), for comparing the electrical resistance of the ferromagnetic layers in said first memory element with the electrical resistance of the ferromagnetic layers in said second memory element, thereby reading the ternary value stored in said memory cell.

10. The magnetoresistive memory device of claim 9, wherein each of said memory elements comprises at least one antiferromagnetic layer (20) for pinning a respective one of said ferromagnetic layers (18) in a certain magnetization state.

11. The magnetoresistive memory device of claim 9, wherein said ferromagnetic layers (30 and 34) have different coercivities.

12. The magnetoresistive memory device of claim 9, wherein said writing electrode (12) of said first memory element (42) and said writing electrode (12) of said second memory element (44) are coupled in series.

13. The magnetoresistive memory device of claim 9, comprising a plurality of memory cells (36) as described in claim 9, disposed in an array having rows and columns, and further comprising:

a plurality of first signal lines (66) disposed in respective rows, coupling said write access circuit (38) to said memory cells;
a plurality of second signal lines (68) disposed in respective columns, coupling said write access circuit to said memory cells;
a plurality of third signal lines (70) disposed in respective rows, coupling said read access circuit (40) to said memory cells;
a plurality of fourth signal lines (72) disposed in respective columns, coupling said read access circuit to said memory cells; and
a plurality of fifth signal lines (74) disposed in respective columns, coupling said read access circuit to said memory cells; wherein
said write access circuit supplies said current to the writing electrode of an arbitrary one of said memory cells through a corresponding one of said first signal lines and a corresponding one of said second signal lines.

14. The magnetoresistive memory device of claim 13, wherein in each of said memory cells (36), the ferromagnetic layers of said first memory element (42) and the ferromagnetic layers of said second memory element (44) are both coupled to a single one of said third signal lines (70), the ferromagnetic layers of said first memory element are coupled to one of said fourth signal lines (72), and the ferromagnetic layers of said second memory element are coupled to one of said fifth signal lines (74).

15. The magnetoresistive memory device of claim 14, wherein said read access circuit reads the ternary value stored in an arbitrary one of said memory cells (36) by supplying a certain current to a corresponding one of said third signal lines (70) and comparing resulting voltages on a corresponding one of said fourth signal lines (72) and a corresponding one of said fifth signal lines (74).

16. The magnetoresistive memory device of claim 14, wherein said read access circuit reads the ternary value stored in an arbitrary one of said memory cells (36) by supplying a certain voltage to a corresponding one of said third signal lines (70) and comparing resulting currents on a corresponding one of said fourth signal lines (72) and a corresponding one of said fifth signal lines (74).

17. A magnetoresistive memory device for storing binary information in an array of rows and columns, comprising:

a plurality of first signal lines (78) disposed in respective rows;
a plurality of second signal lines (80) disposed in respective columns;
a plurality of third signal lines (82) disposed in respective rows;
a plurality of fourth signal lines (84) disposed in respective columns;
a plurality of memory elements (76) disposed at intersections of respective rows and columns, each of said memory elements separately having at least two ferromagnetic layers (14 and 18, or 30 and 34) electrically coupled to one of said third signal lines and one of said fourth signal lines, that collectively exhibit one electrical resistance when magnetized in a parallel state and a different electrical resistance when magnetized in an antiparallel state, and each of said memory elements separately having a writing electrode (12) electrically coupled to a corresponding one of said first signal lines and a corresponding one of said second signal lines, for the passage of a current generating a magnetic field capable of switching said ferromagnetic layers between said parallel state and said antiparallel state;
a write access circuit coupled to said first signal lines and said second signal lines, for supplying current to the writing electrode in an arbitrary one of said memory elements, responsive to said binary information, thereby storing a first binary value by setting the ferromagnetic layers in said one of Said memory elements to said parallel state, and storing a second binary value by setting the ferromagnetic layers in said

one of said memory elements to said antiparallel state; and

a read access circuit coupled to said third signal lines and said fourth signal lines, for detecting the electrical resistance of the ferromagnetic layers in said memory elements, thereby reading the binary information stored in said memory elements.

18. The magnetoresistive memory device of claim 17, wherein each of said memory elements (76) comprises at least one antiferromagnetic layer (20) for pinning a respective one of said ferromagnetic layers (18) in a certain magnetization state.

19. The magnetoresistive memory device of claim 17, wherein said ferromagnetic layers (30 and 34) have different coercivities.

20. The magnetoresistive memory device of claim 17, wherein said read access circuit reads the binary value stored in an arbitrary one of said memory elements (76) by supplying a certain current to a corresponding one of said third signal lines (82) and detecting a resulting voltage on a corresponding one of said fourth signal lines (84).

21. The magnetoresistive memory device of claim 17, wherein said read access circuit reads the binary value stored in an arbitrary one of said memory elements (76) by supplying a certain voltage to a corresponding one of said third signal lines (82) and detecting a resulting current on a corresponding one of said fourth signal lines (84).

22. A method of storing and reading binary information in a magnetoresistive memory cell having a first memory element (42) and a second memory element (44), each of these memory elements separately having at least two ferromagnetic layers (14 and 18, or 30 and 34) that collectively exhibit one electrical resistance when magnetized in a parallel state and a different electrical resistance when magnetized in an antiparallel state, and each of these memory elements separately having a writing electrode (12) for the passage of a current generating a magnetic field capable of switching said ferromagnetic layers between said parallel state and said antiparallel state, comprising the steps of:

storing a first binary value in said memory cell by supplying to the writing electrode of said first memory element a current that sets the ferromagnetic layers in said first memory element to said parallel state and supplying to the writing electrode of said second memory cell a current that sets the ferromagnetic layers in said second memory element to said antiparallel state; storing a second binary value in said memory cell by supplying to the writing electrode of said first memory element a current that sets the ferromagnetic layers in said first memory element to said antiparallel state and supplying to the writing electrode of said second memory cell a current that sets the ferromagnetic layers in said second memory element to said parallel state; and

reading the binary value stored in said memory cell by comparing the electrical resistance of said first memory element with the electrical resistance of said second memory element.

23. The method of claim 22 wherein, in said step of storing a first binary value and said step of storing a second binary value, a single current is supplied to both the writing electrode (12) of said first memory element (42) and the writing electrode (12) of said second memory element (44), these writing electrodes being coupled in series.

24. The method of claim 22, wherein said step of reading comprises the further steps of:

supplying parallel currents to said first memory element (42) and said second memory element (44); and

comparing voltages produced by passage of said parallel currents through said first memory element and said second memory element.

25. The method of claim 22, wherein said step of reading comprises the further steps of:

supplying equal voltages to said first memory element (42) and said second memory element (44); and

comparing resulting currents flowing through said first memory element and said second memory element.

26. A method of storing and reading ternary information in a magnetoresistive memory cell having a first memory element (42) and a second memory element (44), each of these memory elements separately having at least two ferromagnetic layers (14 and 18, or 30 and 34) that collectively exhibit one electrical resistance when magnetized in a parallel state and a different electrical resistance when magnetized in an antiparallel state, and each of these memory elements separately having a writing electrode (12) for the passage of a current generating a magnetic field capable of switching said ferromagnetic layers between said parallel state and said antiparallel state, comprising the steps of:

storing a first ternary value in said memory cell by supplying to the writing electrode of said first memory element a current that sets the ferro-

magnetic layers of said first memory element to said parallel state and supplying to the writing electrode of said second memory cell a current that sets the ferromagnetic layers of said second memory element to said antiparallel state;
storing a second ternary value in said memory cell by supplying to the writing electrode of said first memory element a current that sets the ferromagnetic layers of said first memory element to said antiparallel state and supplying to the writing electrode of said second memory cell a current that sets the ferromagnetic layers of said second memory element to said parallel state;
storing a third ternary value in said memory cell by supplying to the writing electrode of said first memory element and the writing electrode of said second memory element currents that set the ferromagnetic layers of both said first memory element and said second memory element to identical states among said parallel state and said antiparallel state; and
reading the binary value stored in said memory cell by comparing the electrical resistance of said first memory element with the electrical resistance of said second memory element.

27. The method of claim 26, comprising the further step of:

initializing said memory cell by supplying to the writing electrode (12) of said first memory element (42) a current that sets the ferromagnetic layers of said first memory element to said parallel state and supplying to the writing electrode (12) of said second memory cell (44) a current that sets the ferromagnetic layers of said second memory element to said parallel state.

28. The method of claim 26 wherein, in said step of storing a first ternary value, said step of storing a second ternary value, and said step of storing a third ternary value, a single current is supplied to both the writing electrode (12) of said first memory element (42) and the writing electrode (12) of said second memory element (44), these writing electrodes being coupled in series.

29. The method of claim 26, wherein said step of reading comprises the further steps of:

supplying parallel currents to said first memory element (42) and said second memory element (44); and
comparing voltages produced by passage of said parallel currents through said first memory element and said second memory element.

30. The method of claim 26, wherein said step of reading comprises the further steps of:

supplying equal voltages to said first memory element (42) and said second memory element (44); and
comparing resulting currents flowing through said first memory element and said second memory element.

31. A method of storing and reading binary information in a memory element having at least two ferromagnetic layers (14 and 18, or 30 and 34) that collectively exhibit one electrical resistance when magnetized in a parallel state and a different electrical resistance when magnetized in an antiparallel state, and having a writing electrode (12) for the passage of a current generating a magnetic field capable of switching said ferromagnetic layers between said parallel state and said antiparallel state, comprising the steps of:

storing a first binary value in said memory element by supplying to said writing electrode a current that, by itself, sets the ferromagnetic layers in said memory element to said parallel state;
storing a second binary value in said memory element a current that, by itself, sets the ferromagnetic layers in said memory element to said antiparallel state; and
reading the binary value stored in said memory element by detecting the electrical resistance of said ferromagnetic layers.

32. The method of claim 31, wherein said step of reading comprises the further steps of:

supplying a certain current to said memory element; and
detecting a voltage produced by passage of said current through said memory element.

33. The method of claim 31, wherein said step of reading comprises the further steps of:

supplying a certain voltage to said memory element; and
detecting a current flowing through said memory element.

FIG. 1

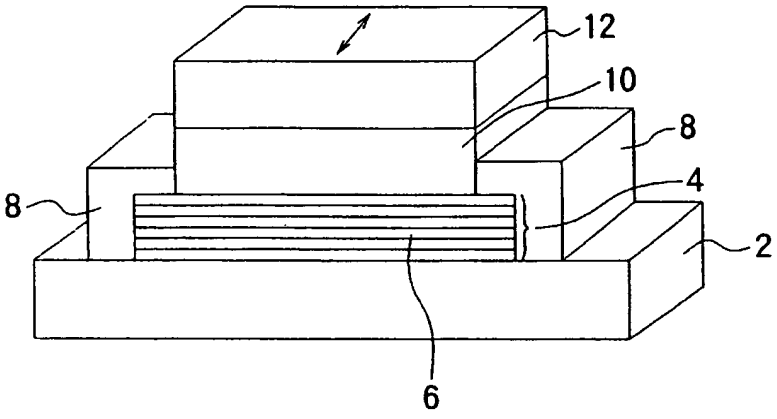


FIG. 2

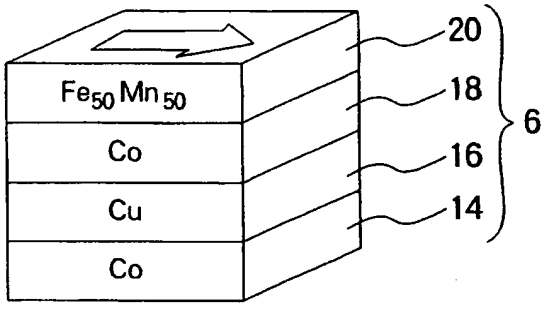


FIG. 3

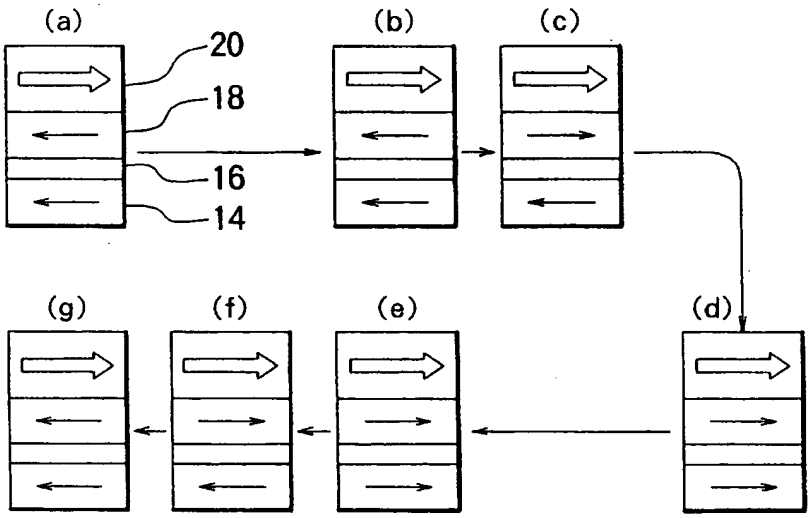


FIG. 4

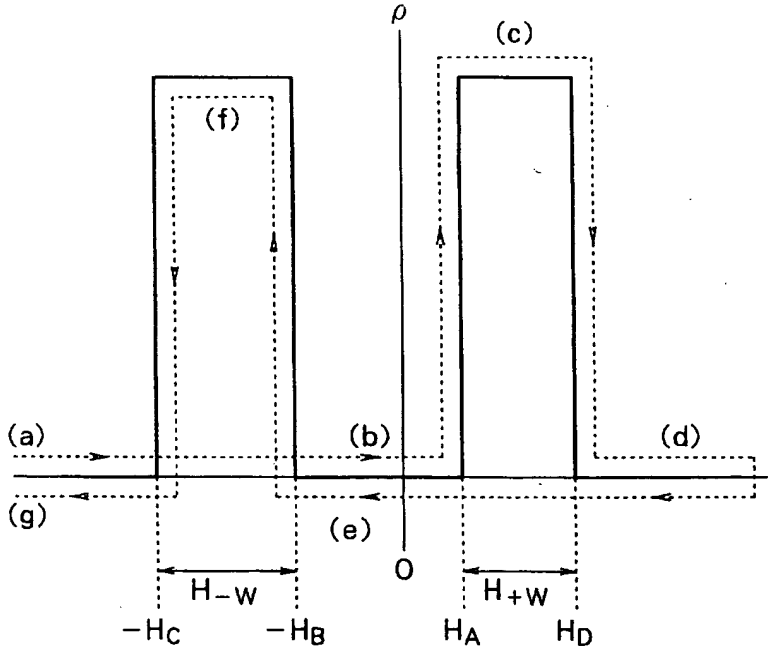
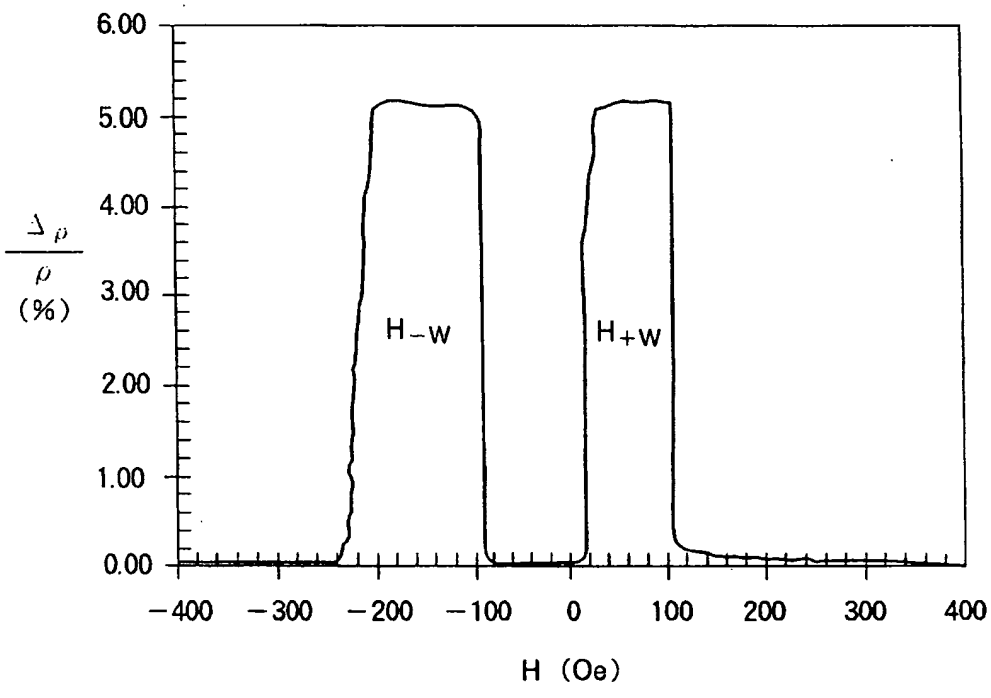


FIG. 5


6.00
5.00
4.00
3.00
2.00
1.00
0.00
Δρ/ρ (%)
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H+W
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−300
−200
−100
0
100
200
300
400
H (Oe)

FIG. 6

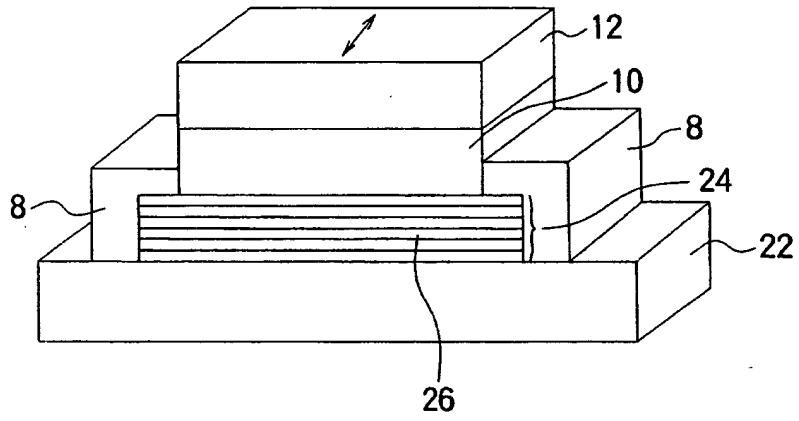


FIG. 7

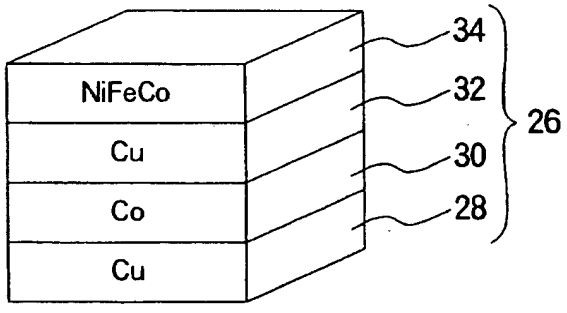


FIG. 8

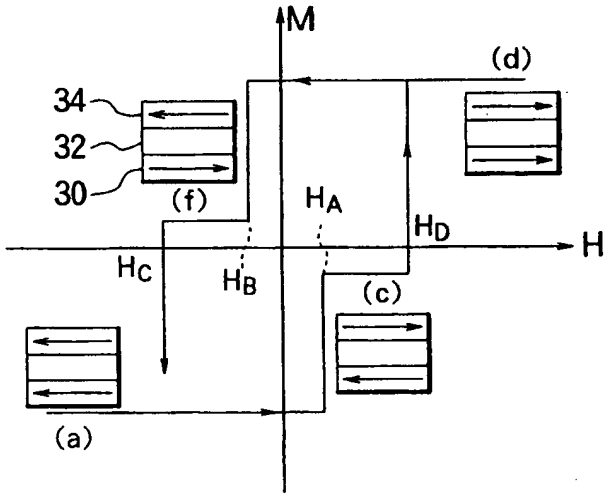


FIG. 9

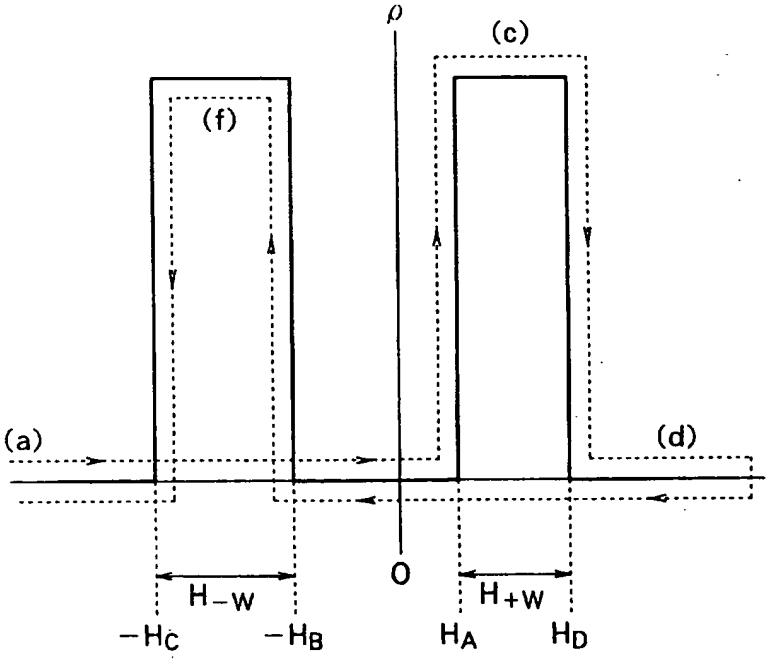
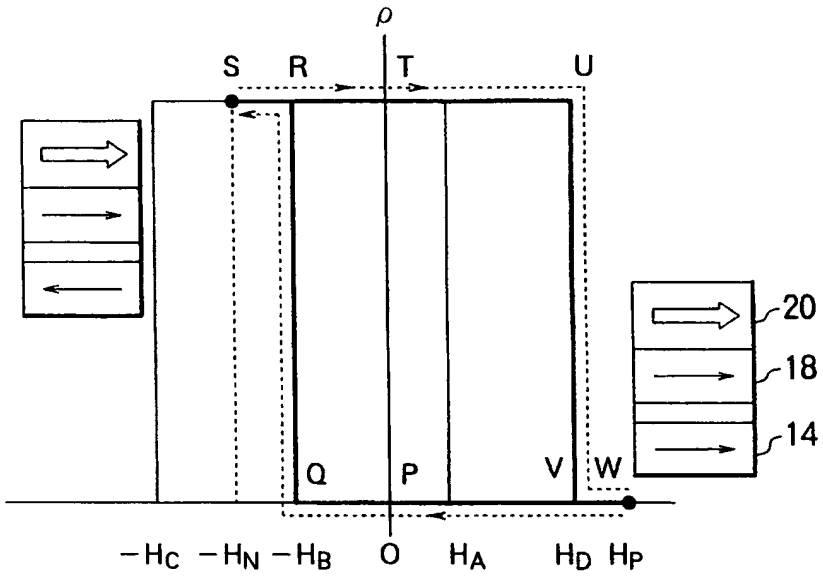


FIG. 10


ρ
S
R
T
U
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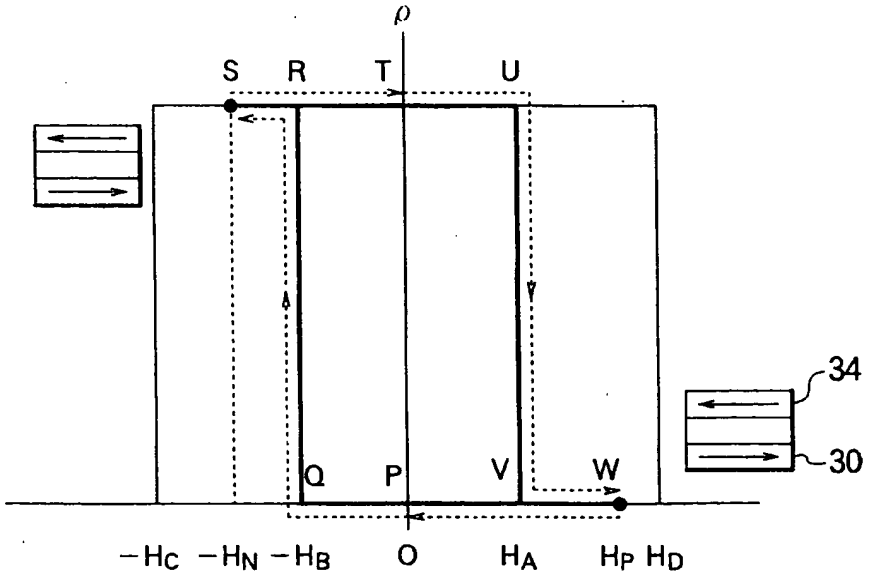
18
14
Q
P
V
W
−HC
−HN
−HB
O
HA
HD
HP

FIG. 11


ρ
S
R
T
U
34
30
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P
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HA
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HD

FIG. 12

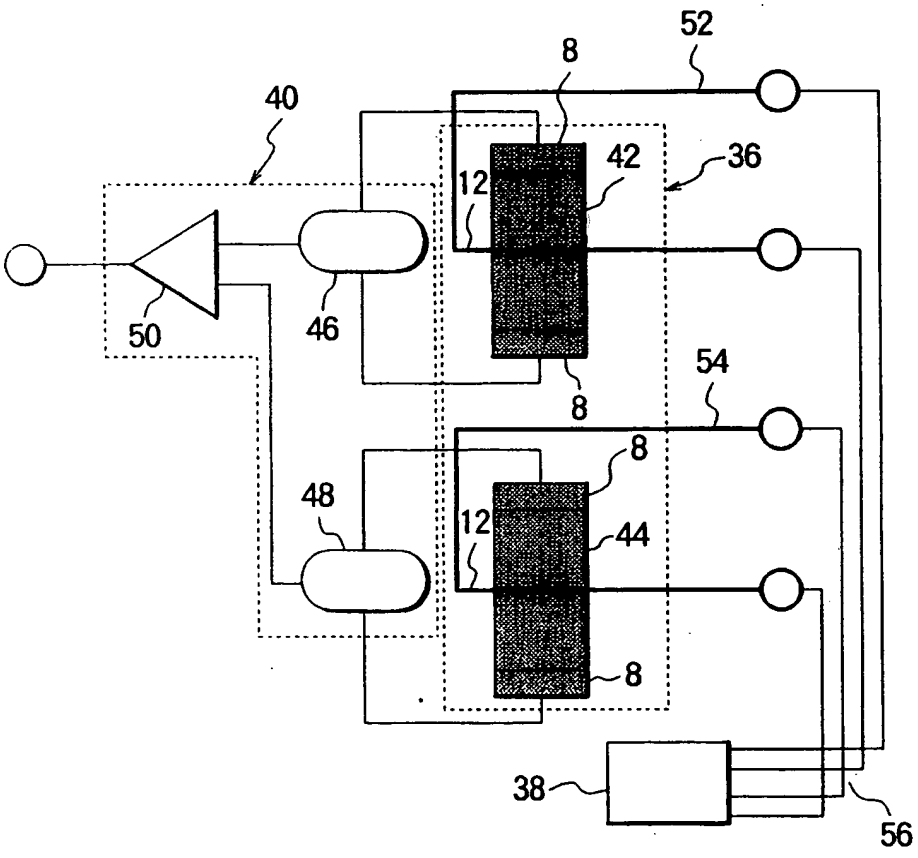


FIG. 13

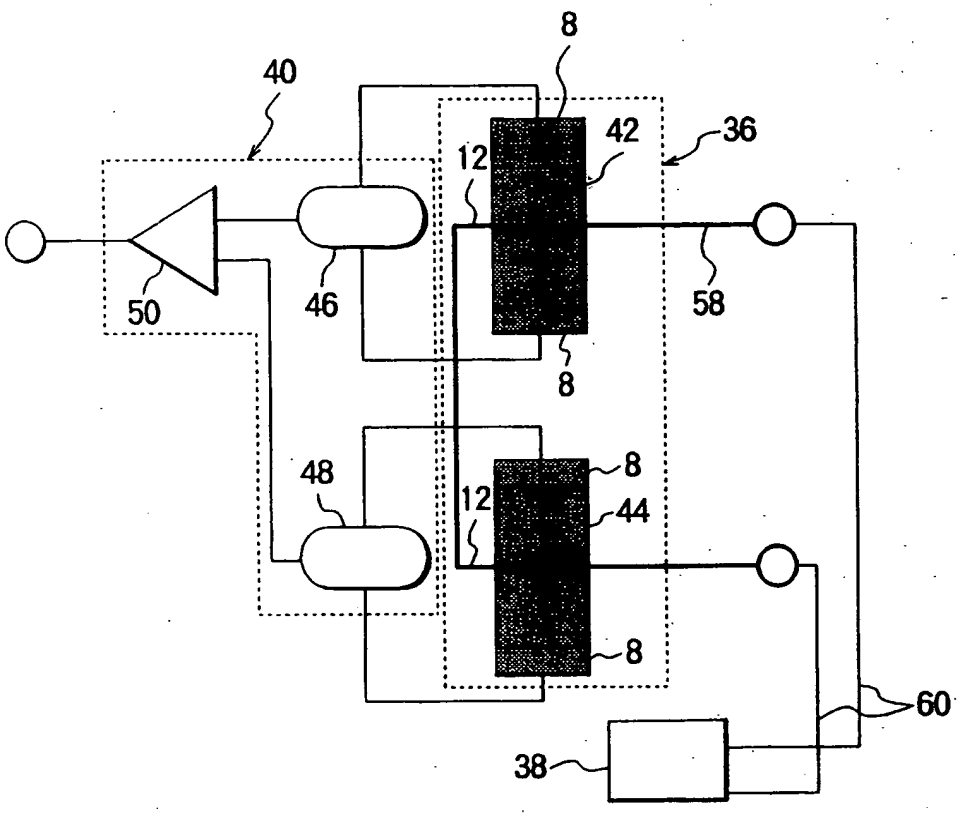


FIG. 14

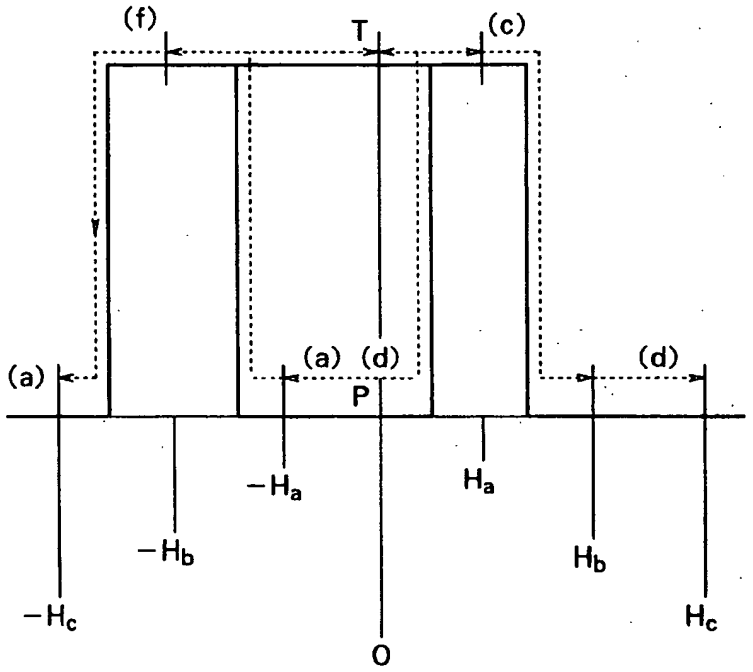


FIG. 15

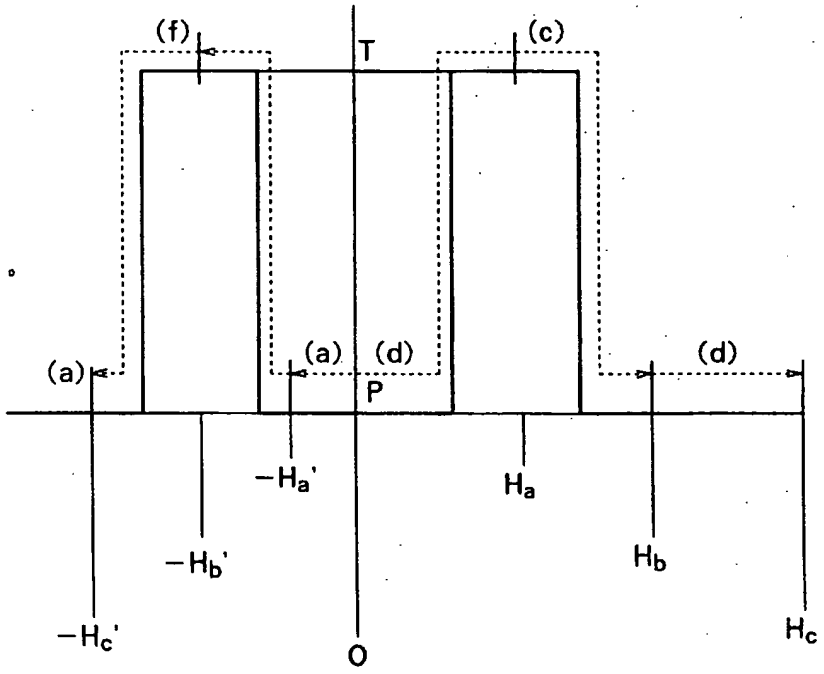


FIG. 16

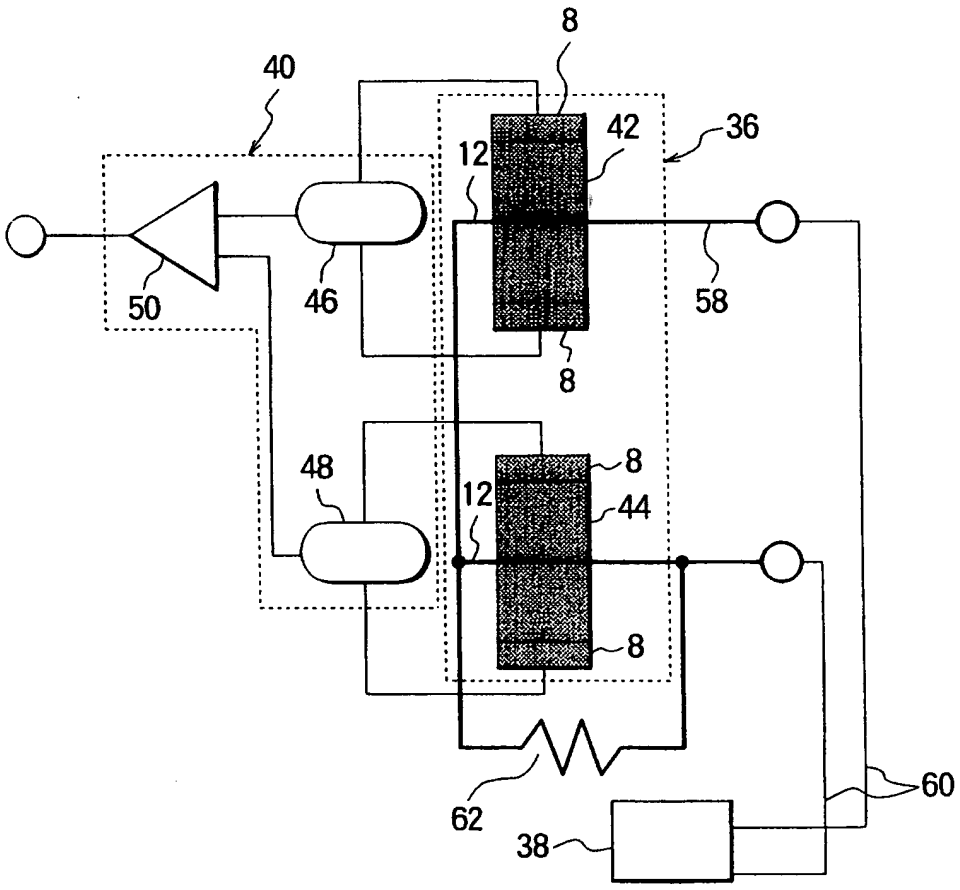
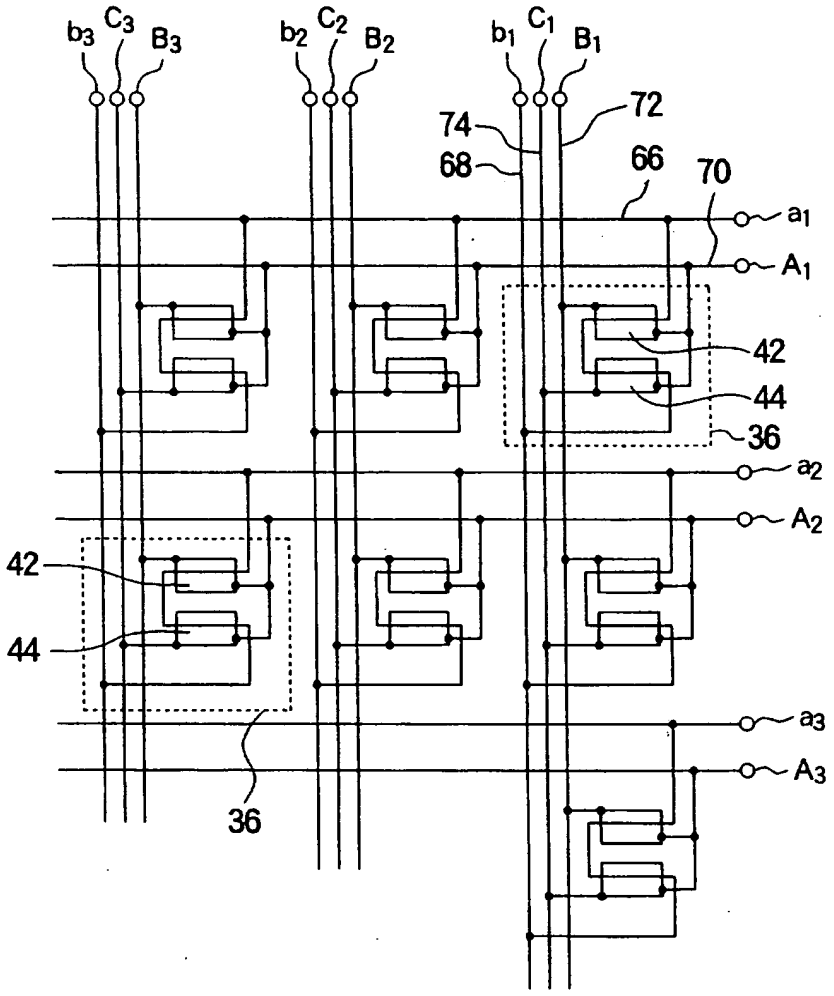


FIG. 17


b3
C3
B3
b2
C2
B2
b1
C1
B1
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A1
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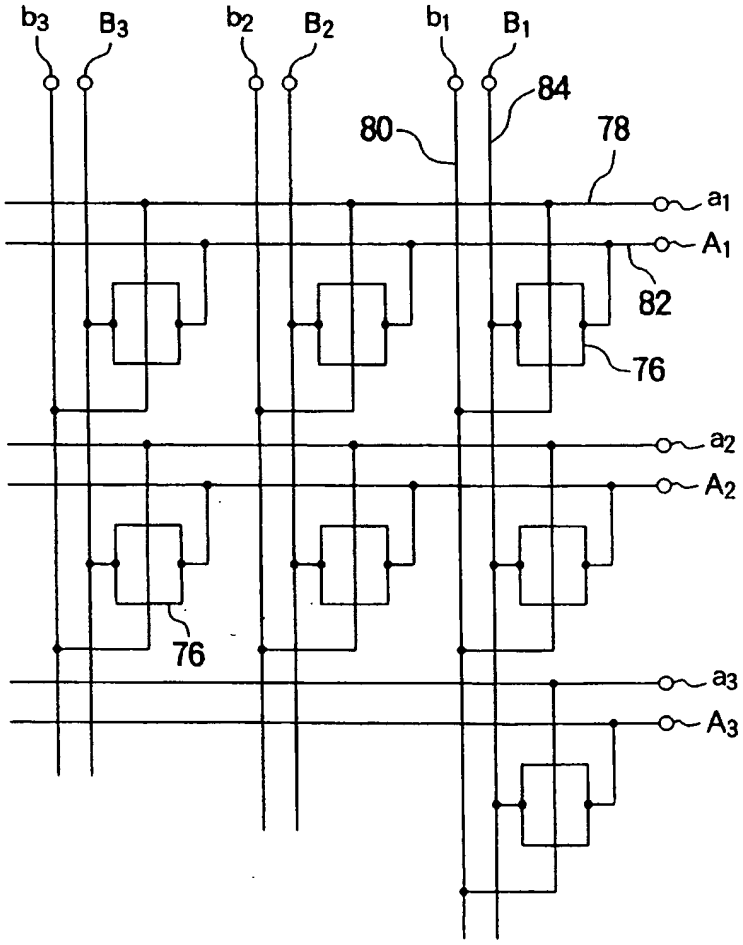
a2
A2
42
44
36
a3
A3

FIG. 18



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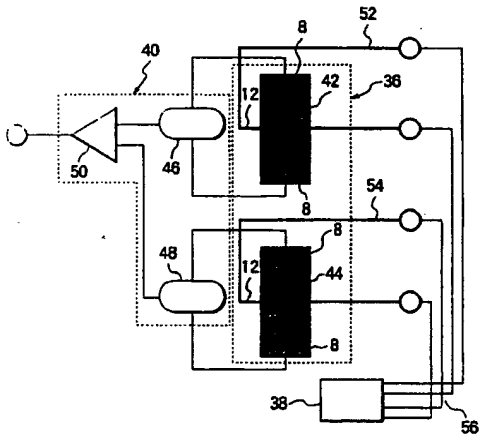
(54) High-speed, low current magnetoresistive memory device

(57) A memory cell has two magnetoresistive memory elements, each with at least two ferromagnetic layers. The electrical resistance of each memory element differs depending on whether the ferromagnetic layers are magnetized in the parallel or antiparallel state. Binary information is stored in the memory cell by supplying currents that generate magnetic fields setting one memory element to the parallel state and the other memory element to the antiparallel state. Alternatively, ternary information is stored, two of the ternary values being stored in the same way as the binary values, and the third ternary value being stored by setting both memory elements to the same state. The stored values are read by comparing the resistances of the two memory elements.

FIG. 12



EP 0 773 551 A3

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EUROPEAN SEARCH REPORT

Application Number
EP 96 11 8209

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
D,A	EP 0 613 148 A (IBM) 31 August 1994 * the whole document *	1-33	G11C11/15
A	US 4 751 677 A (DAUGHTON JAMES M ET AL) 14 June 1988 * the whole document *	1-33	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

G11C

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	9 September 1998	Beasley-Suffolk, D

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